WHAT IS CLAIMED IS:

1. A computer system comprising:

a driver interface;

a receiver interface coupled to said driver interface via interconnect, said interconnect comprising a plurality of traces of varying lengths; and

a programmable delay element coupled to said driver interface, said delay element being programmed to delay switching of output signals of said driver interface by a delay corresponding to a length of a trace traveled by a respective signal.

2. The computer system of claim 1, wherein said delay is inversely proportional to said length.

3. The computer system of claim 1, wherein said delay is proportional to a difference between said length and a length of a longest trace.

4. The computer system of claim 1, wherein said receiver interface is wider than said driver interface.

5. The computer system of claim 1, wherein said driver interface is coupled to a memory controller, and said receiver interface is coupled to memory.

6. The computer system of claim 1, said delay element comprising a plurality of variable delay outputs selectably coupled to each of a plurality of output latches of said driver interface.

7. The computer system of claim 1, wherein no delay is introduced in a signal connected to a longest trace.

8. The computer system of claim 1, wherein said delay element is a delay locked loop.

9. A computer system comprising:

a plurality of output latches of a first interface;

interconnect coupling said output latches to a second interface and comprising a plurality of traces of varying lengths, said traces being configured to propagate signals from said output latches to said second interface;

a plurality of multiplexers, each multiplexer coupled between a latch of said output latches and a delay element comprising a plurality of variable delay outputs; and

a plurality of programmable registers, each register coupled to a multiplexer of said multiplexers, said registers being programmable to select one of said plurality of variable delay outputs in accordance with a length of a trace that propagates a signal of said latch.

10. The computer system of claim 9, said plurality of variable delay outputs comprising a clock signal and phase-shifted versions of said clock signal.

11. The computer system of claim 9, wherein said first interface is coupled to a memory controller, and said second interface is coupled to memory.

12. A method comprising:

connecting a first interface to a second interface with interconnect comprising traces configured to propagate signals, said traces having varying lengths; and

programming a delay element to delay signals output by said first interface for propagation to said second interface by a delay corresponding to respective lengths of traces propagating said output signals.

13. The method of claim 12, further comprising:

providing a plurality of variable delay outputs from said delay element; and

selecting one of said plurality in accordance with a length of a trace of said traces.

14. The method of claim 12, wherein said delay is inversely proportional to said respective lengths.

15. The method of claim 12, wherein said delay is proportional to a difference between said respective lengths and a length of a longest trace.

16. The method of claim 12, wherein said programming is performed by software.

17. The method of claim 16, wherein said software is a BIOS program.

18. An interconnect for a computer system, comprising:

a plurality of traces, each having a respective length;

a plurality of programmable delay outputs, each provided on a terminal end of one of the traces, and characterized by a delay corresponding to a difference between the length of the respective trace and the length of a longest trace.

19. The interconnect of claim 18, wherein no delay output is provided for the longest trace.

20. A computer system comprising:

first and second agents; and

an interconnect coupled to the first and second agents and comprising:

a plurality of traces, each having a respective length; and

a plurality of delay outputs, each provided on a terminal end of one of the traces, and characterized by a programmable delay corresponding to a difference between the length of the respective trace and the length of a longest trace.

21. The computer system of claim 20, wherein said terminal end is at a receiver interface of either of said first and second agents.

22. A method comprising:

generating a multi-bit data signal at a first agent;

outputting the multi-bit data signal to a plurality of traces, one bit per trace;

programming a delay for the signals on a plurality of traces, each by an amount corresponding to a difference between a length of a respective trace and a length of a longest trace; and

thereafter, receiving the data signal at a second agent.

23. The method of claim 22, wherein said delay is inversely proportional to a length of a respective trace.

24. A computer system comprising:

a receiver interface coupled to interconnect comprising a plurality of traces of varying lengths; and

a programmable delay element coupled to said receiver interface, said delay element being programmable to delay sampling of received signals of said receiver interface by a delay corresponding to a length of a trace traveled by a received signal.

25. The computer system of claim 24, wherein said delay element comprises a plurality of multiplexers, each multiplexer coupled between a buffer of said interface and a plurality of variable delay outputs; and

a plurality of programmable registers, each register coupled to a multiplexer of said multiplexers, said registers being programmable to select one of said plurality of variable delay outputs in accordance with a length of a trace traveled by a received signal.

26. A method comprising:

connecting a receiver interface to interconnect comprising traces configured to propagate signals, said traces having varying lengths; and

programming a delay element to delay signals received at said

receiver interface by a delay corresponding to respective lengths of traces propagating said received signals.

27. The method of claim 26, further comprising:

providing a plurality of variable delay outputs from said delay element; and

selecting one of said plurality in accordance with a length of a trace of said traces.

28. The method of claim 26, wherein said delay is directly proportional to said respective lengths.

29. The method of claim 26, wherein said programming is performed by software.

30. The method of claim 29, wherein said software is a BIOS program.